NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPD7720
DIGITAL SIGNAL PROCESSOR

Description

The NEC μPD7720 Signal Processing Interface (SPI) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the SPI to efficiently implement signal processing functions in a wide range of environments and applications.

The NEC SPI is the state of the art in signal processing today, and for the future.

Applications

- ☐ Speech Synthesis and Analysis
- ☐ Digital Filtering
- ☐ Fast Fourier Transforms (FFT)
- ☐ Dual-Tone Multi-Frequency (DTMF) Transmitters/Receivers
- ☐ High Speed Data Modems
- ☐ Equalizers
- ☐ Adaptive Control
- ☐ Sonar/Radar Image Processing
- ☐ Numerical Processing

Performance Benchmarks

☐ Second Order Digital Filter (Biquad)	2.25 μs
☐ Sine/Cos of Angles	5.25 μs
☐ μ/A Law to Linear Conversion	0.50 μs
☐ FFT: 32-point Complex	0.7 ms
64-point Complex	1.6 ms

Features

- ☐ Fast Instruction Execution — 250 ns
- ☐ 16-Bit Data Word
- ☐ Multi-Operation Instructions for Optimizing Program Execution
- ☐ Large Memory Capacities

Program ROM	512 x 23 Bits
Data ROM	510 x 13 Bits
Data RAM	128 x 16 Bits

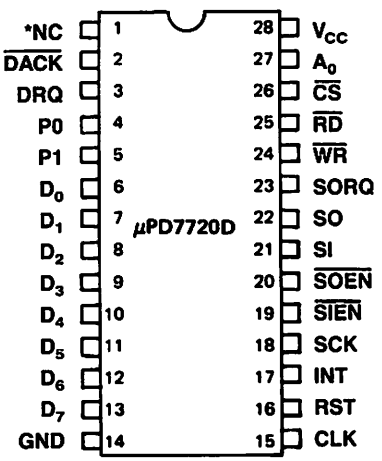
- ☐ Fast (250 ns) 16 x 16 31-Bit Multiplier
- ☐ Dual Accumulators
- ☐ Four Level Subroutine Stack for Program Efficiency
- ☐ Multiple I/O Capabilities
  - Serial
  - Parallel
  - DMA
- ☐ Compatible with Most Microprocessors, Including:
  - μPD8080
  - μPD8085
  - μPD8086
  - μPD780 (Z80)™*
- ☐ Power Supply +5V
- ☐ Technology NMOS
- ☐ Package — 28 Pin Dip

*Z80 is a registered trademark of Zilog Corporation.

Pin Identification

Pin No.	Symbol	I/O	Function
1	NC	I	No Connection for masked ROM μPD7720. Consult μPD77P20 specifications for connection for pin-compatible EPROM version.
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the Data Bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request. Signals that the μPD7720 is requesting a data transfer on the Data Bus.
4, 5	P_0, P_1	O	General purpose output control lines.
6-13	D_0-D_7	I/O Three-state	Port for data transfer between the Data Register or Status Register and external Data Bus.
14	GND		Ground.
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset. Initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin executes a call instruction to location 100H, if interrupts were previously enabled.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. Enables the shift clock to the Serial Input Register.
20	$\overline{SOEN}$	I	Serial Output Enable. Enables the shift clock to the Serial Output Register.
21	SI	I	Serial Data Input. Inputs 8- or 16-bit serial-data words from an external device such as an A/D converter.
22	SO	O Three-state	Serial Data Output. Outputs 8- or 16-bit data words to an external device such as a D/A converter.
23	SORQ	O	Serial Data Output Request. Specifies to an external device that the Serial Data Register has been loaded and is ready for output. SORQ is reset when the entire 8- or 16-bit word has been transferred.
24	$\overline{WR}$	I	Write Control Signal. Writes an input from the data port into the Data Register.
25	$\overline{RD}$	I	Read Control Signal. Reads an output to the data port from the Data or Status Register.
26	$\overline{CS}$	I	Chip Select. Enables data transfer through data port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects Data Register for Read/Write (low) or Status Register for read (high).
28	V_{CC}		+5V Power

Pin Configuration



*No connection, μPD7720.
Must be connected for EPROM version; consult μPD77P20 specifications.

Rev/3

Functional Description

Fabricated in high speed NMOS, the μPD7720 SPI is a complete 16-bit microcomputer on a single chip. ROM space is provided for program and coefficient storage, while the on-chip RAM may be used for temporary data, coefficients, and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 x 16-bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 ns instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughput. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional microprocessors. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand-alone microcomputer.

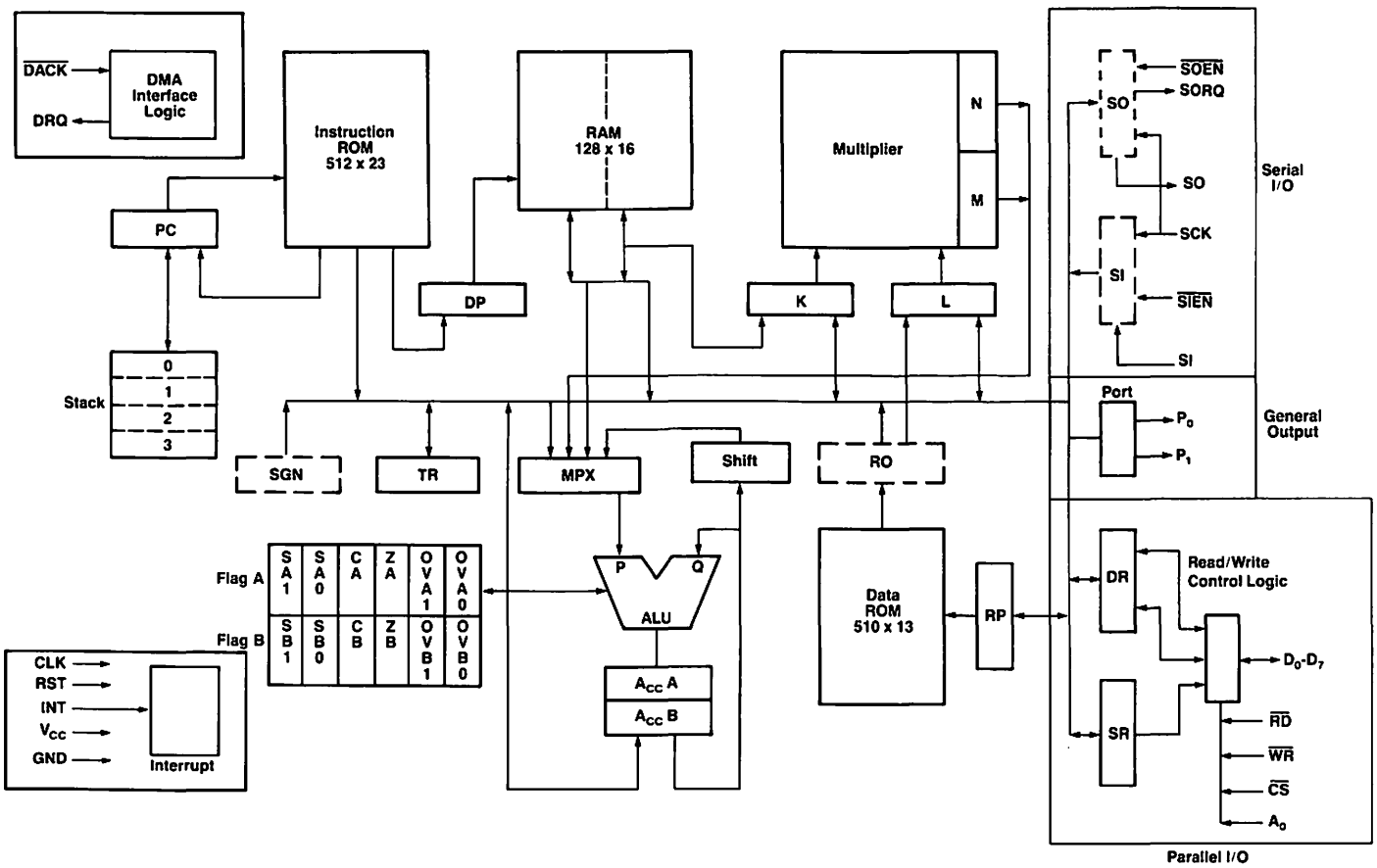
Memory

Memory is divided into three types: Program ROM, Data ROM, and Data RAM. The 512 x 23-bit words of Program ROM are addressed by a 9-bit Program Counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The Data ROM is organized in 510 x 13-bit words which are addressed through a 9-bit ROM pointer (RP register). The RP may be modified simultaneously with arithmetic instructions so that the next value is available for the next instruction. The Data ROM is ideal for storing the necessary coefficients, conversion tables, and other constants for your processing needs.

The Data RAM is 128 x 16-bit words and is addressed through a 7-bit data pointer (DP register). The DP has extensive addressing features that operate simultaneously with arithmetic instructions so that no added time is taken for addressing or address modification.

Block Diagram



Arithmetic Capabilities

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and a data move between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as three successive additions or subtractions.

ACC A/B Flag Registers

Flag A	SA1	SA0	CA	ZA	OVA1	OVA0
Flag B	SB1	SB0	CB	ZB	OVB1	OVB0

Sign Register (SGN)

When OVA1 (or OVB1) is set, the SA1 (or SB1) bit will hold the corrected sign of the overflow. The SGN Register will use SA1 (SB1) to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated value.

Multiplier

Thirty-one bit results are developed by a 16 x 16-bit 2's complement multiplier in 250 ns. The result is automatically latched to two 16-bit registers M&N (sign and 15 higher bits in M, 15 lower bits in N; LSB in N is zero) at the end of each instruction cycle. A new product is available for use after every instruction cycle, providing significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

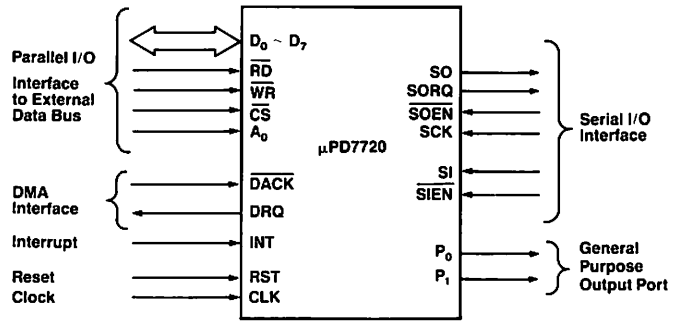
Interrupt

A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0, thus disabling the interrupt facilities until reenabled under program control.

Input/Output

General

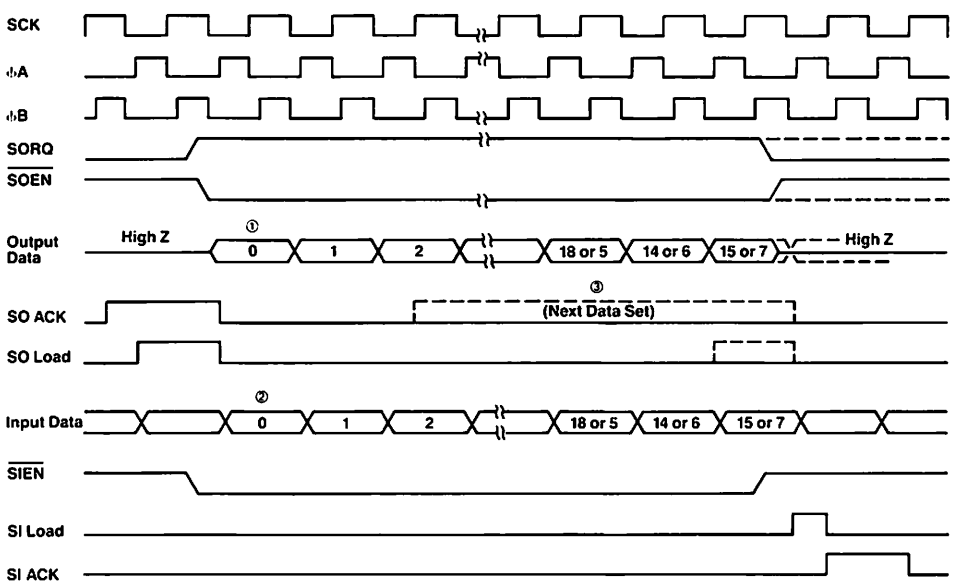
The NEC SPI has three communication ports; two serial and one 8-bit parallel, each with its own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and $\overline{DACK}$) for high speed data transfer and reduced processor overhead. A general purpose 2-line output port rounds out a full complement of interface capability.



Serial I/O

The two shift registers (SI, SO) are software-configurable to single or double byte transfers. The shift registers are externally clocked (SCK) to provide a simple interface between the SPI and serial peripherals such as A/D and D/A converters, codecs, or other SPIs.

Serial I/O Timing



Notes: ① Data clocked out on falling edge of SCK.
② Data clocked in on rising edge of SCK.
③ Broken line denotes consecutive sending of next data.

Parallel I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085, and 8086 processor buses and may be used with other processors and computer systems.

Parallel R/W Operation

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Operation
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels
X	X	1	1	
0	0	0	1	Data from D_0-D_7 are latched to DR ①
0	0	1	0	Contents of DR are output to D_0-D_7 ①
0	1	0	1	Illegal (SR is read only)
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal (May not read and write simultaneously)

Note: ① Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS). The condition of $\overline{DACK}$ = 0 is equivalent to A_0 = $\overline{CS}$ = 0.

Status Register (SR)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RQM	USF1	USF0	DRS	DMA	DRC	SOC	SIC	EI	0	0	0	0	0	P1	P0

The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

Status Register Flags

Flag	Description
RQM (Request for Master)	A read or write from DR to IDB sets RQM = 1. An external read (write) resets RQM = 0.
USF1 and USF0 (User Flags 1 and 0)	General purpose flags which may be read by an external processor for user defined signaling.
DRS (DR Status)	For 16-bit DR transfers (DRC = 0). DRS = 1 after first 8 bits have been transferred DRS = 0 after all 16 bits transferred.
DMA (DMA Enable)	DMA = 0 (Non-DMA transfer mode) DMA = 1 (DMA transfer mode).
DRC (DR Control)	DRC = 0 (16-bit mode) DRC = 1 (8-bit mode).
SOC (SO Control)	SOC = 0 (16-bit mode) SOC = 1 (8-bit mode).
SIC (SI Control)	SIC = 0 (16-bit mode) SIC = 1 (8-bit mode).
EI (Enable Interrupt)	EI = 0 (interrupts disabled) EI = 1 (interrupts enabled).
P1, P0 (Ports 0 and 1)	P0 and P1 directly control the state of output pins P0 and P1.

Instructions

The SPI has 3 types of instructions, all of which are one 23-bit word and execute in 250 ns.

Arithmetic/Move-Return (OP = 00/RT = 01)

	22 21	20 19	18 17 16 15	14	13 12	11 10 9	8	7 6 5 4	3 2 1 0
OP	0 0	P-Select	ALU	ASL	DP_L	DP_H-M	RPDCR	SRC	DST
RT	0 1	Same as OP instruction							

OP/RT Instruction Field Specification

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 2. The ALU functions operate on the value specified by the P-select field. (See Table 1.)

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 7 and 8 respectively). The difference in the two instructions of this type is that RT executes a subroutine or interrupt return at the end of the instruction cycle while the OP does not.

Table 1. P-Select Field

Mnemonic	D_{20}	D_{19}	ALU Input
RAM	0	0	RAM
IDB	0	1	Internal Data Bus ①
M	1	0	M Register
N	1	1	N Register

Note: ① Any value on the on-chip data bus. Value may be selected from any of the registers listed in Table 7 source register selections.

Table 2. ALU Field

						Flags	SA1	SA0	CA	ZA	OVA1	OVA0
Mnemonic	D_{18}	D_{17}	D_{16}	D_{15}	ALU Function		SB1	SB0	CB	ZB	OVB1	OVB0
NOP	0	0	0	0	No Operation		–	–	–	–	–	–
OR	0	0	0	1	OR		X	↕	0	↕	0	0
AND	0	0	1	0	AND		X	↕	0	↕	0	0
XOR	0	0	1	1	Exclusive OR		X	↕	0	↕	0	0
SUB	0	1	0	0	Subtract		↕	↕	↕	↕	↕	↕
ADD	0	1	0	1	ADD		↕	↕	↕	↕	↕	↕
SBB	0	1	1	0	Subtract with Borrow		↕	↕	↕	↕	↕	↕
ADC	0	1	1	1	Add with Carry		↕	↕	↕	↕	↕	↕
DEC	1	0	0	0	Decrement A_{CC}		↕	↕	↕	↕	↕	↕
INC	1	0	0	1	Increment A_{CC}		↕	↕	↕	↕	↕	↕
CMP	1	0	1	0	Complement A_{CC} (1's Complement)		X	↕	0	↕	0	0
SHR1	1	0	1	1	1-bit R-Shift		X	↕	↕	↕	0	0
SHL1	1	1	0	0	1-bit L-Shift		X	↕	↕	↕	0	0
SHL2	1	1	0	1	2-bit L-Shift		X	↕	0	↕	0	0
SHL4	1	1	1	0	4-bit L-Shift		X	↕	0	↕	0	0
XCHG	1	1	1	1	8-bit Exchange		X	↕	0	↕	0	0

Notes: ↕ May be affected, depending on the results.
– Previous status can be held.
0 Reset.
X Indefinite.

Table 3. ASL Field

Mnemonic	D_{14}	A_{CC} Selection
ACCA	0	A_{CC} A
ACCB	1	A_{CC} B

Table 4. DP_L Field

Mnemonic	D_{13}	D_{12}	Low DP Modify (DP_3-DP_0)
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 5. DP_H-M Field

Mnemonic	D_{11}	D_{10}	D_9	High DP Modify
M0	0	0	0	Exclusive OR of DP_H (DP_6-DP_4) with the Mask defined by the three bits (D_{11}-D_9) of the DP_H-M field
M1	0	0	1	
M2	0	1	0	
M3	0	1	1	
M4	1	0	0	
M5	1	0	1	
M6	1	1	0	
M7	1	1	1	

Table 6. RPDCR Field

Mnemonic	D_8	RP Operation
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Table 7. SRC Field

Mnemonic	D_7	D_6	D_5	D_4	Source Register
NON	0	0	0	0	No Register
A	0	0	0	1	A_{CC} A (Accumulator A)
B	0	0	1	0	A_{CC} B (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR No Flag ①
SR	1	0	1	0	SR Status Register
SIM	1	0	1	1	SI Serial In MSB ②
SIL	1	1	0	0	SI Serial In LSB ③
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

Notes: ① DR to IDB, RQM not set. In DMA, DRQ not set.
② First bit in goes to MSB, last bit to LSB.
③ First bit in goes to LSB, last bit to MSB (bit reversed).

Table 8. DST Field

Mnemonic	D_3	D_2	D_1	D_0	Destination Register
@NON	0	0	0	0	No Register
@A	0	0	0	1	A_{CC} A (Accumulator A)
@B	0	0	1	0	A_{CC} B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB ①
@SOM	1	0	0	1	SO Serial Out MSB ②
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K, ROM → L ③
@KLM	1	1	0	0	Hi RAM → K, IDB → L ④
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	No Register
@MEM	1	1	1	1	RAM

Notes: ① LSB is first bit out.
② MSB is first bit out.
③ Internal data bus to K and ROM to L register.
④ Contents of RAM address specified by DP_6 = 1, (i.e., 1, DP_5, DP_4-DP_0) is placed in K register. IDB is placed in L.

Jump/Call/Branch

JP Instruction Field Specification

	22 21	20 19 18	17 16 15 14 13	12 11 10 9 8 7 6 5 4	3 2 1 0
JP	10	BRCH	CND	NA	

Three types of program counter modifications are accommodated by the processor and are listed in Table 9. All the instructions, if unconditional or if the specified condition is true, take their next program execution address from the Next Address field (NA); otherwise PC = PC + 1.

Table 9. BRCH Field

D_{20}	D_{19}	D_{18}	Branch Instruction
1	0	0	Unconditional jump
1	0	1	Subroutine call
0	1	0	Conditional jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 10 lists all the instruction mnemonics of the Jump/Call/Branch codes.

Load Data (LDI)

LD Instruction Field Specification

22 21	20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
LD	11	ID / DST

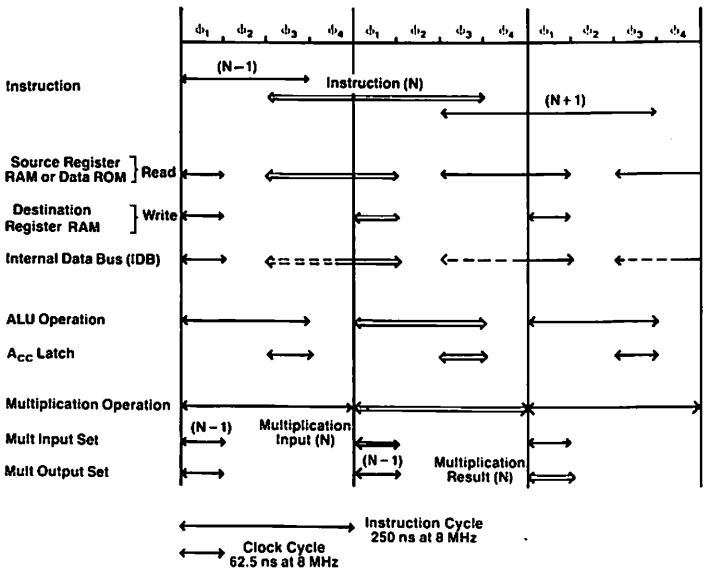
The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 8).

Table 10. BRCH/CND Fields

Mnemonic	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	Conditions①
JMP	1	0	0	0	0	0	0	0	No Condition
CALL	1	0	1	0	0	0	0	0	No Condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 0
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	DP_L = 0
JDPLF	0	1	0	1	1	0	0	1	DP_L = F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

Note: ① BRCH or CND values not in this table are prohibited.

Instruction Timing (Four Phase-Internal Clock)



Instruction Timing

To control the execution of instructions, the external 8-MHz clock is divided into a four-phase, nonoverlapping clock. Execution begins at the rising edge of $\phi 3$ and ends at the falling edge of $\phi 2$. The ALU commences operation at the rise of $\phi 1$, and completes all operations at the fall of $\phi 3$.

Once an instruction-ROM address is available at the rise of $\phi 3$, the instruction is latched, and the source register and RAM address are determined so that data may be put on the internal bus by the fall of $\phi 4$. The ALU input is latched at the rise of $\phi 1$, and the output is available for accumulator latch at the rise of $\phi 3$. The cycle then repeats.

The multiplier takes its input at the rise of $\phi 1$, and its results are available in 250 ns, at the rise of the next $\phi 1$.

Absolute Maximum Ratings*

T_a = 25°C	
Voltage (V_{CC} Pin)	−0.5 to +7.0V ①
Voltage, Any Input	−0.5 to +7.0V ①
Voltage, Any Output	−0.5 to +7.0V ①
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C

Note: ① With respect to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V\phi_L$	−0.5		0.45	V	
CLK High Voltage	$V\phi_H$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 µA
Input Load Current	I_{LIL}			−10	µA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	µA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	µA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}			10	µA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		180	280	mA	

Capacitance

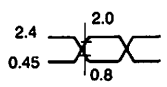
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK Input Capacitance	$C\phi$			20	pF	
Input Pin Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Output Pin Capacitance	C_{OUT}			20	pF	

AC Characteristics

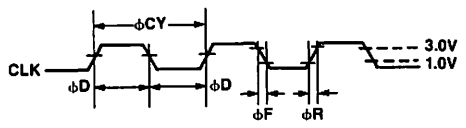
T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Time	ϕCY	122		2000	ns	①
CLK Pulse Width	ϕD	60			ns	
CLK Rise Time	ϕR			10	ns	①
CLK Fall Time	ϕF			10	ns	①
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Read to Data Floating	t_{DF}	10		100	ns	C_L = 100 pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250			ns	②
DRQ Delay	t_{AM}			150	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1			ϕD	②
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	①
SORQ Delay	t_{DRQ}	30		150	ns	C_L = 100 pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30			ns	
SO Delay from SCK = LOW	t_{DCK}			150	ns	
SO Delay from SCK with SORQ ↑	t_{DZRQ}	20		300	ns	②
SO Delay from SCK	t_{DZSC}	20		300	ns	②
SO Delay from $\overline{SOEN}$	t_{DZE}	20		160	ns	②
$\overline{SOEN}$ to SO Floating	t_{HZE}	20		200	ns	②
SCK to SO Floating	t_{HZSC}	20		300	ns	②
SO Delay from SCK with SORQ ↓	t_{HZRQ}	70		300	ns	②
$\overline{SIEN}$, SI Setup Time	t_{DC}	55			ns	②
$\overline{SIEN}$, SI Hold Time	t_{CD}	30			ns	
P_0, P_1 Delay	t_{DP}			ϕCY +150	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

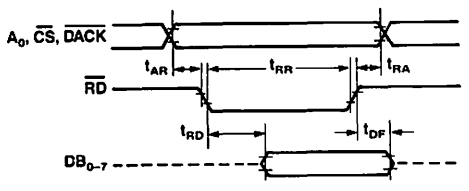
Notes: ① Voltage at measuring point of timing 1.0V and 3.0V
② Voltage at measuring point of AC Timing
$V_{IL} = V_{OL} = 0.8V$
$V_{IH} = V_{OH} = 2.0V$
Input Waveform of AC Test (except CLK, SCK)



Timing Waveforms

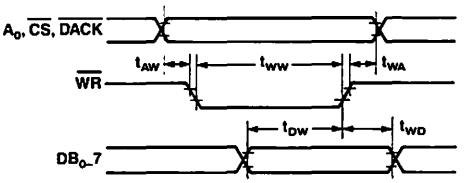


READ Operation

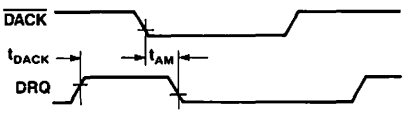


Timing Waveforms (Cont.)

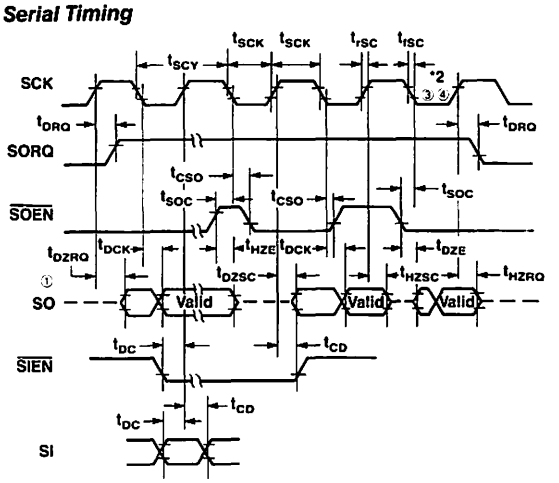
WRITE Operation



DMA Operation



Serial Timing



Notes: ① For SO timing, the data at rising edge of SCK is valid and the other data is invalid. In set-up hold time of data for SCK, the most strict specifications are the following:
setup = $t_{SCK} - t_{DCK}$
hold = t_{HZRQ}
② Voltage at measuring point of t_{rsc} and t_{fsc} for SCK timing:
③3.0V ④1.0V

Development Tools

For software development, editing, debugging, and assembly into object code, the NDS Development System, designed and manufactured by NEC Electronics U.S.A. Inc., is available. The ASM77 Cross-Assembler and SIM77 Simulator for analyzing development code and I/O timing characteristics are available for both the NDS and for other systems supporting CP/M (®Digital Research Corp.) or ISIS-II (®Intel Corp.) operating systems. Additionally, the ASM77 Cross-Assembler is offered in Fortran for VAX systems under VMS (®Digital Equipment Corp.).

Once software development is complete, the code can be completely evaluated and debugged in hardware with the Evakit-7720 Evaluation System. The Evakit provides true in-circuit real time emulation of the SPI for debugging and demonstrating your final system design. Code may be down-loaded to the Evakit from a development system via an RS232 port. The Evakit also serves to program the μPD77P20, a full-speed EPROM version of the SPI. A demonstration mask ROM chip, containing some common digital filtering routines, including N-stage IIR (biquadratic) and FIR (transversal) filters, is available to test hardware interfaces to the SPI.

Further operational details of the SPI can be found in the μPD7720 Signal Processing Interface Technical Manual. Operation of the SPI development tools is described in the Cross-Assembler User Manual, the Simulator Operating Manual, the Evakit-7720 Operation Manual, and the NEC Development Systems Users' Manual.

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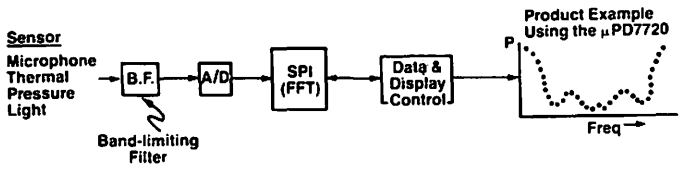
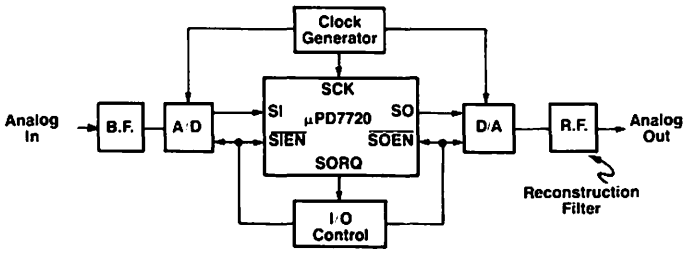
One Natick Executive Park
Natick, Massachusetts 01760
TEL 617-655-8833
TWX 710-386-2110

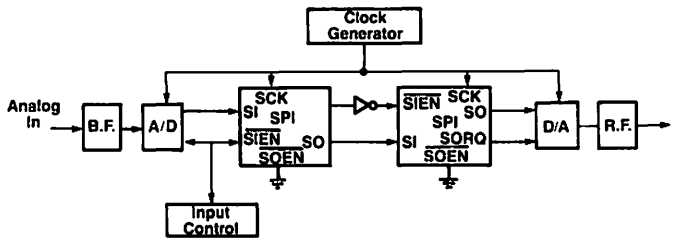
Spectrum Analysis System



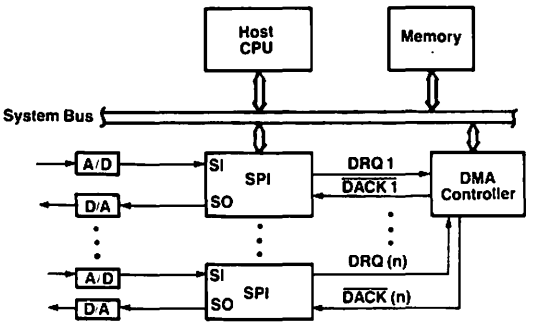
An Analog-to-Analog Digital Processing System Using a Single SPI



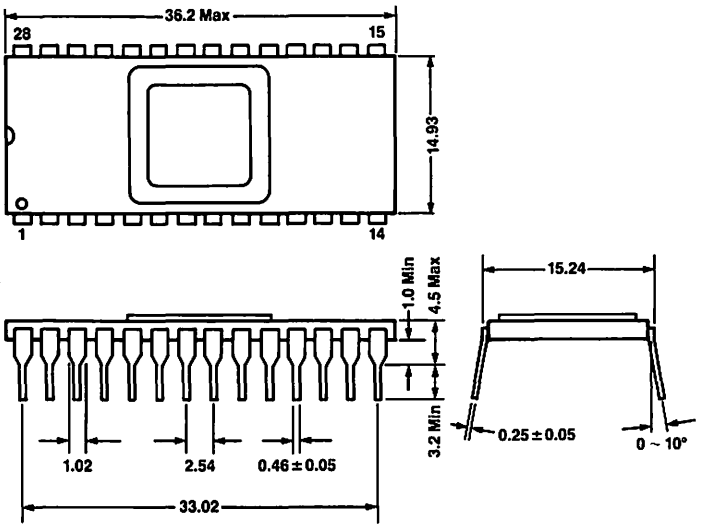
A Signal Processing System Using Cascaded SPIs & Serial Communication



A Signal Processing System Using SPI(s) as a Complex Computer Peripheral



Package Dimensions (Millimeters)



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